MEMORY

UNCLASSIFIED

RISK ASSESSMENT: *Low*

SAFETY CONSIDERATIONS:

Electrical Shock Hazard

Electrostatic Discharge

ENVIRONMENTAL CONSIDERATIONS:

None

TERMINAL LEARNING OBJECTIVE

ACTION: Identify the different memory operations.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on Memory operations.

ENABLING LEARNING OBJECTIVE

ACTION: Identify the physical characteristics of memory.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on Memory operations.

MEMORY

Located outside of the Microprocessor. (main and mass memory)

A collection of sequential locations each with its own unique address.

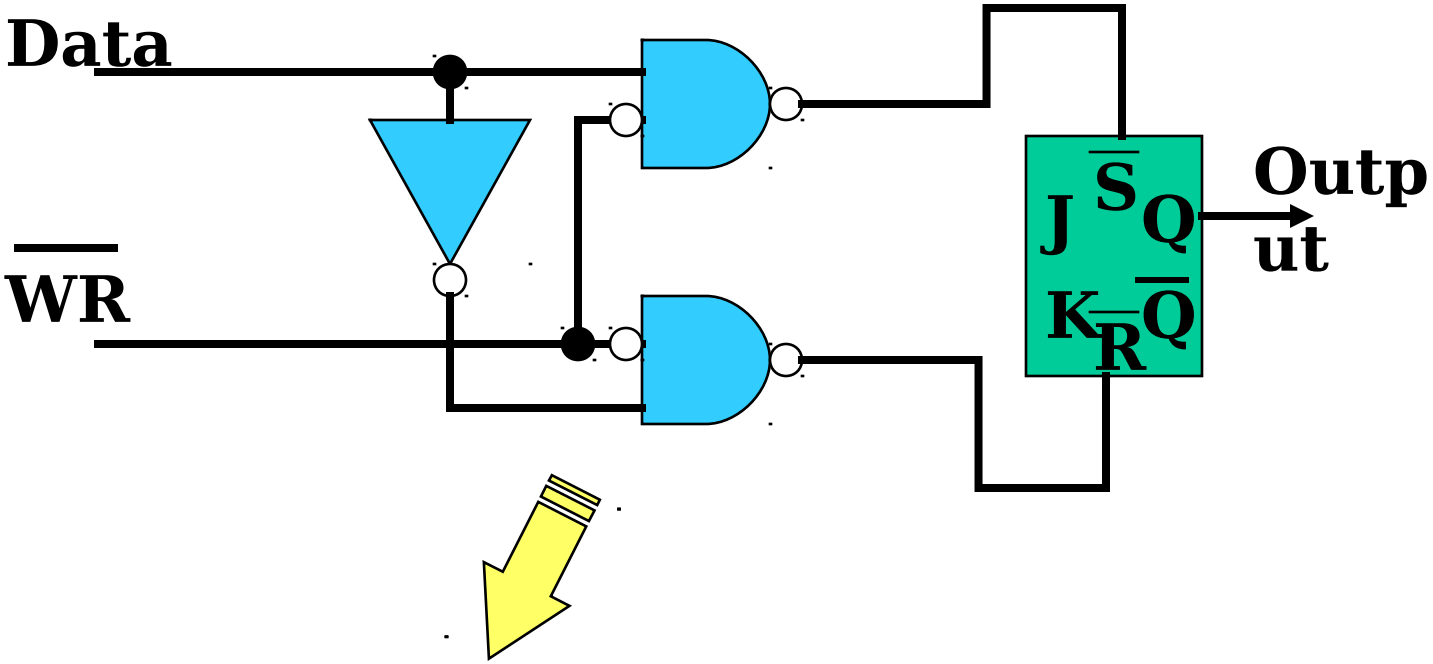
Stores large groups of binary data.

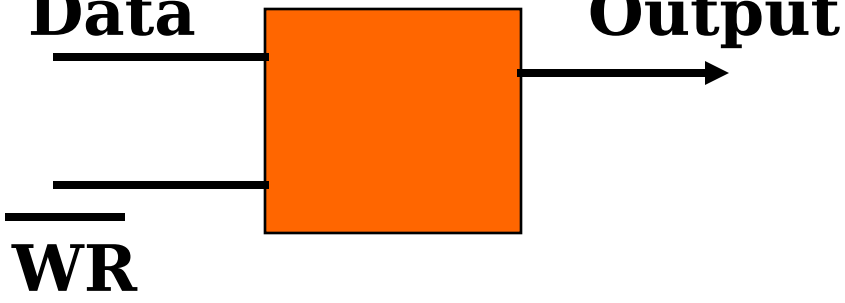
MEMORY CELL

A device that holds one of two states. 1 or 0.

It holds these states as either +5v or 0v.

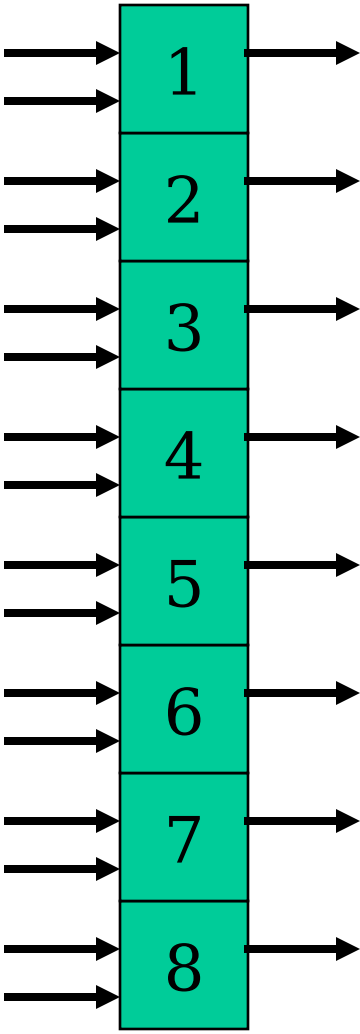
These states remain stable.





Basic Memory Cell

Cell Organization



MEMORY CELL

Cells are arranged in rows of 8.

Each location holds 8 bits / 1 byte.

Data is ready for reading at all times.

But…it should only be read when the write signal is high.

ENABLING LEARNING OBJECTIVE

ACTION: Identify the types of memory.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on Memory operations.

RAM

RANDOM ACCESS MEMORY

Read from or write to RAM.

Data is lost when power is removed.

The NIDA-500 uses static RAM chips U14 & U15.

Arranged in blocks of 8 X 32,768 bits each chip for a total of 8 X

RAM

RANDOM ACCESS MEMORY

Two types of RAM - Static and Dynamic.

Static RAM is made up of Flip/Flops.

Dynamic RAM is made of Capacitors.

Static RAM

Dynamic RAM

Stable & fast.

Takes up space little space

Leaks.

Uses

ROM

READ ONLY MEMORY

Two EPROM’s - U12 & U13 - can be erased and reprogrammed.

Programs are stored by the manufacturer. (monitor and initialization programs)

Non-volatile.

ROM

READ ONLY MEMORY

Each cell is made up of isolated capacitors.

Leakage is minimal.

Over years or elevated temperatures the charge may be lost.

ROM addresses are available from F0000 - FFFFF. (A16 - A19 high).

ENABLING LEARNING OBJECTIVE

ACTION: Identify Random Access Memory (RAM) operations.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on Memory operations.

RAM

CONTROL PINS

CHIP SELECT - CS - uses $\overline{\text{RAMSEL}}$.

OUTPUT ENABLE - OE - uses $\overline{\text{MEMRD}}$.

WRITE ENABLE - WE - uses $\overline{\text{MWRHI}}$ & $\overline{\text{MWRLO}}$

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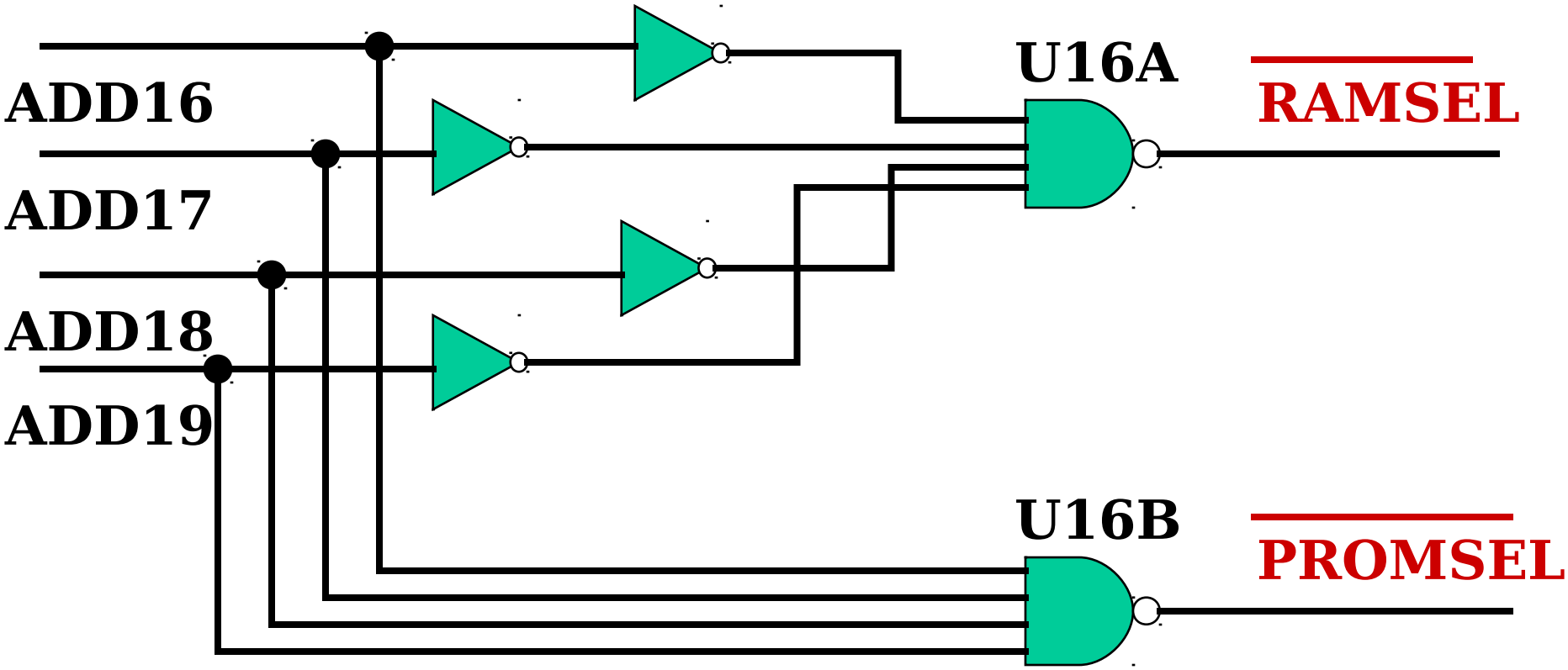

Chip select RAM / ROM

ADD16 - ADD19 all low selects RAM.

ADD16 - ADD19 all high selects ROM.

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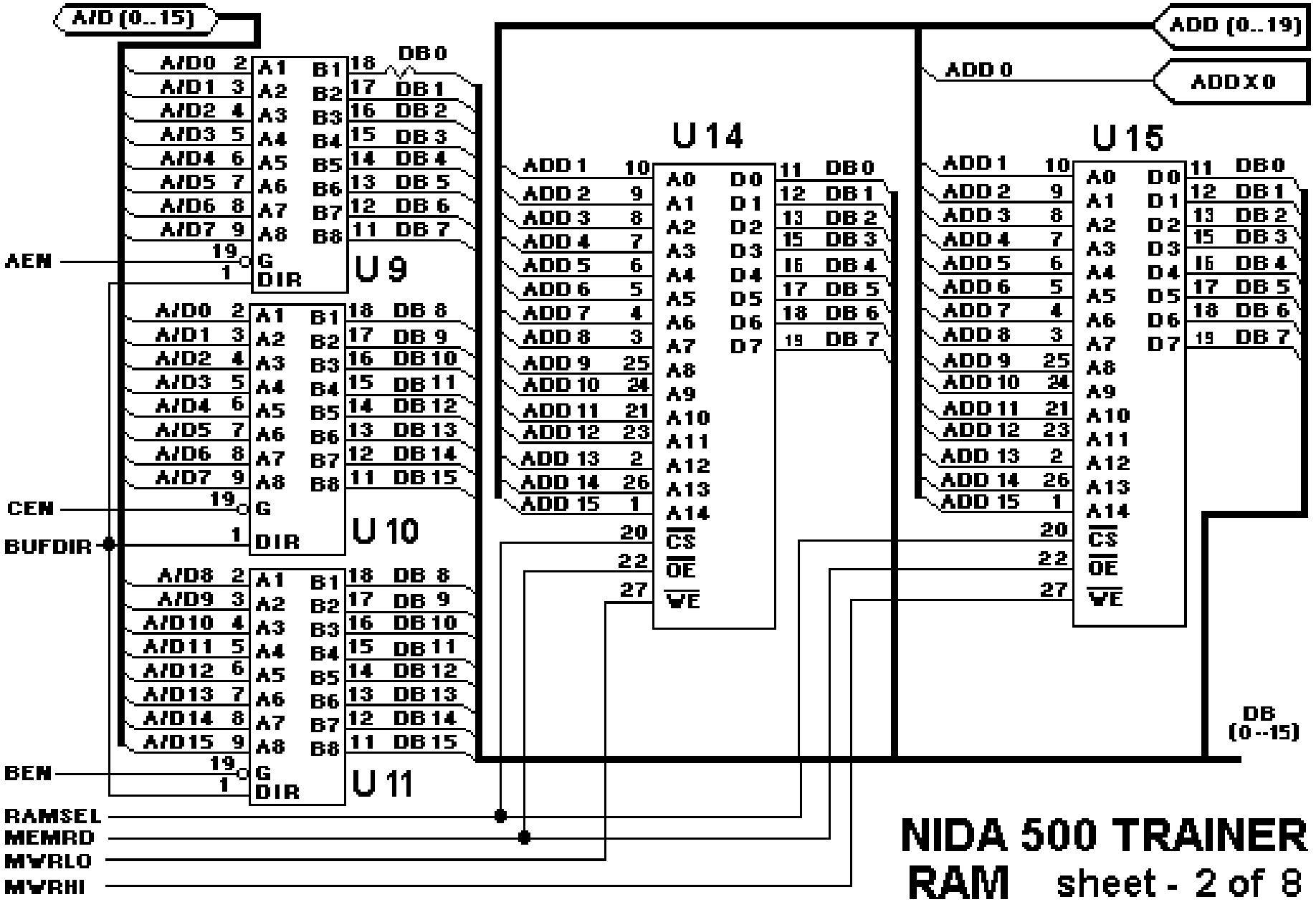
A/D (0..15)
ADD (0..19)
ADD 0
ADDX0
DB0
U 9
U 10
U 11
U 14
U 15
AEN
CEN
BUFDIR
BEN
RAMSEL
MEMRD
MWRLO
MWRHI
DB (0--15)
NIDA 500 TRAINER
RAM sheet - 2 of 8

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RAM DATA PINS

8 Bits of parallel data - D0 - D7 that are bi-directional.

U14 - low byte. U15 - high byte.

RAM ADDRESS PINS

15 Pins on each chip used for addressing. The possible combinations are:

000 0000 0000 0000 - 111 1111 1111 1111 (0000 - 7FFF) —over 32,000 locations per chip.

ADD0 is used in conjunction with UBE to select the low byte, high

Byte Selection Chart

$\overline{\text{UBE}}$	ADD0	Characteristics
0	0	Whole Word
0	1	Upper byte
1	0	Lower byte
1	1	None

ENABLING LEARNING OBJECTIVE

ACTION: Identify Erasable Programmable Read Only Memory (EPROM) operations.

CONDITIONS: Given a classroom environment, Computer Aided Instruction (CAI), workstation, NIDA electronic trainer, and official OMEMS reference material.

STANDARDS: Correctly answer 7 of 10 questions on Memory operations.

ROM

CONTROL PINS

CHIP ENABLE - CE uses $\overline{\text{PROMSEL}}$.

OUTPUT ENABLE - $\overline{\text{OE}}$ uses $\overline{\text{MEMRD}}$.

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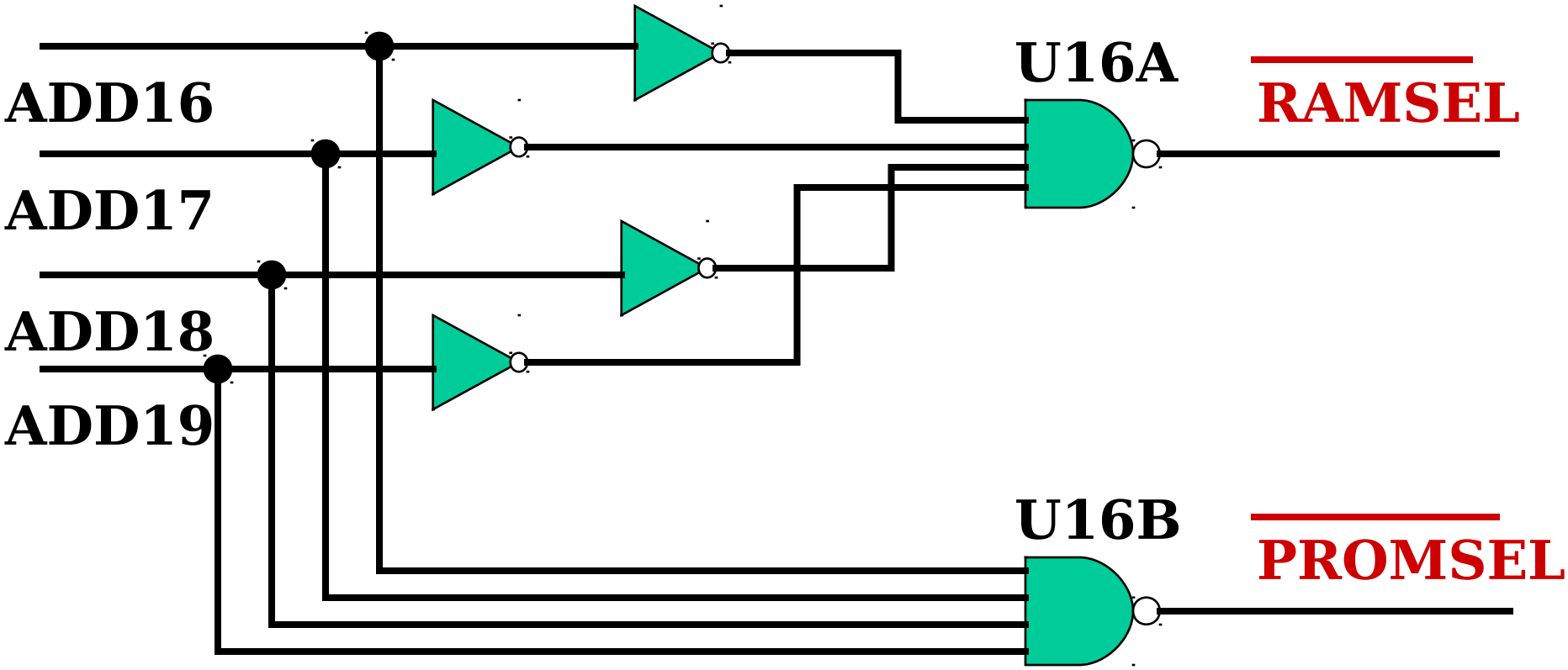

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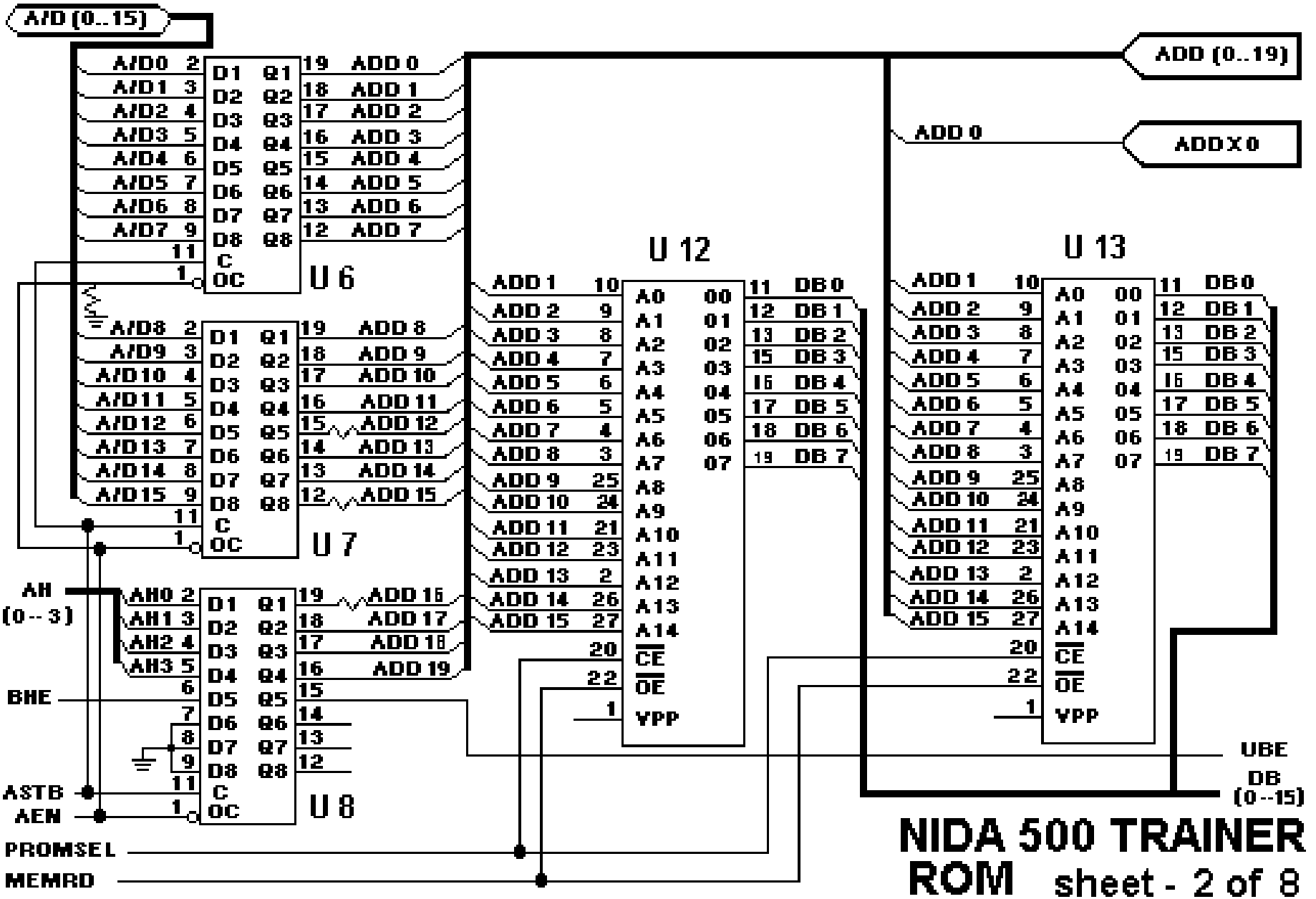
A/D (0..15)
A/D0 2
A/D1 3
A/D2 4
A/D3 5
A/D4 6
A/D5 7
A/D6 8
A/D7 9
11
1
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
D8 Q8
C
OC
19 ADD 0
18 ADD 1
17 ADD 2
16 ADD 3
15 ADD 4
14 ADD 5
13 ADD 6
12 ADD 7
U 6
A/D8 2
A/D9 3
A/D10 4
A/D11 5
A/D12 6
A/D13 7
A/D14 8
A/D15 9
11
1
19 ADD 8
18 ADD 9
17 ADD 10
16 ADD 11
15 ADD 12
14 ADD 13
13 ADD 14
12 ADD 15
U 7
AH
(0 -- 3)
AH0 2
AH1 3
AH2 4
AH3 5
6
7
8
9
11
1
19 ADD 16
18 ADD 17
17 ADD 18
16 ADD 19
15
14
13
12
U 8
BHE
ASTB
AEN
PROMSEL
MEMRD
ADD 1 10
ADD 2 9
ADD 3 8
ADD 4 7
ADD 5 6
ADD 6 5
ADD 7 4
ADD 8 3
ADD 9 25
ADD 10 24
ADD 11 21
ADD 12 23
ADD 13 2
ADD 14 26
ADD 15 27
20
22
1
A0 00
A1 01
A2 02
A3 03
A4 04
A5 05
A6 06
A7 07
A8
A9
A10
A11
A12
A13
A14
CE
OE
VPP
11 DB 0
12 DB 1
13 DB 2
15 DB 3
16 DB 4
17 DB 5
18 DB 6
19 DB 7
U 12
U 13
ADD (0..19)
ADD 0
ADDX 0
UBE
DB
(0 --15)
NIDA 500 TRAINER
ROM sheet - 2 of 8
CF351L06-

ROM DATA PINS

8 Data pins on each chip that are bi-directional. D0 – D7

Since there is no “write enable” the computer cannot write to the ROM, only read.

VPP (Pin 1) is used by the manufacturer for programming the

ROM

ADDRESS PINS

15 Address pins on each chip which allows over 32,000 memory locations.

Byte selection is not needed. 16 bits are always transferred during a memory read function.

SUMMARY

Identified what memory is and how it functions.

Identified the difference between RAM and ROM.

Identified the signals used to control memory.